### Device Usage Page (usage\_statistics\_webtalk.html)

This HTML page displays the device usage statistics that will be sent to Xilinx.

To see the actual file transmitted to Xilinx, please click [here](http://docs.google.com/usage_statistics_webtalk.xml).

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| **software\_version\_and\_target\_device** | | | |
| **beta** | FALSE | **build\_version** | 2086221 |
| **date\_generated** | Wed Mar 27 17:00:51 2019 | **os\_platform** | WIN64 |
| **product\_version** | Vivado v2017.4 (64-bit) | **project\_id** | e29592b29a394e0580c318f5da7dfa7a |
| **project\_iteration** | 14 | **random\_id** | 35b13a06b9f958e59f87537dcf9de47e |
| **registration\_id** | 211464776\_0\_0\_626 | **route\_design** | TRUE |
| **target\_device** | xc7z020 | **target\_family** | zynq |
| **target\_package** | clg484 | **target\_speed** | -1 |
| **tool\_flow** | Vivado |

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| **user\_environment** | | | |
| **cpu\_name** | Intel(R) Core(TM) i5-8250U CPU @ 1.60GHz | **cpu\_speed** | 1800 MHz |
| **os\_name** | Microsoft Windows 8 or later , 64-bit | **os\_release** | major release (build 9200) |
| **system\_ram** | 12.000 GB | **total\_processors** | 1 |

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| **vivado\_usage** | | | |

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| **gui\_handlers** | | | |
| addsrcwizard\_specify\_hdl\_netlist\_block\_design=1 | addsrcwizard\_specify\_simulation\_specific\_hdl\_files=3 | basedialog\_apply=4 | basedialog\_cancel=10 |
| basedialog\_no=1 | basedialog\_ok=140 | basedialog\_yes=12 | closeplanner\_cancel=1 |
| closeplanner\_yes=6 | cmdmsgdialog\_ok=24 | constraintschooserpanel\_create\_file=1 | copyrundialog\_run\_name=3 |
| createconstraintsfilepanel\_file\_name=2 | createsrcfiledialog\_file\_name=7 | exploreaheadview\_launch\_selected\_runs=3 | exploreaheadview\_reset\_selected\_runs=1 |
| expreporttreepanel\_exp\_report\_tree\_table=6 | exprunmenu\_change\_run\_settings=6 | exprunmenu\_launch\_runs=8 | exprunmenu\_launch\_step=2 |
| exprunproppanels\_name=2 | expruntreepanel\_exp\_run\_tree\_table=51 | filesetpanel\_file\_set\_panel\_tree=148 | flownavigatortreepanel\_flow\_navigator\_tree=167 |
| gettingstartedview\_create\_new\_project=2 | gettingstartedview\_open\_project=2 | graphicalview\_zoom\_fit=23 | graphicalview\_zoom\_in=124 |
| graphicalview\_zoom\_out=165 | hpopuptitle\_close=1 | mainmenumgr\_floorplanning=3 | mainmenumgr\_help=2 |
| mainmenumgr\_io\_planning=3 | mainmenumgr\_report=5 | mainmenumgr\_run=4 | mainmenumgr\_timing=3 |
| mainmenumgr\_tools=10 | mainmenumgr\_view=4 | mainmenumgr\_window=2 | mainwinmenumgr\_layout=2 |
| msgtreepanel\_message\_view\_tree=8 | msgview\_information\_messages=3 | pacommandnames\_add\_sources=6 | pacommandnames\_auto\_connect\_target=7 |
| pacommandnames\_auto\_update\_hier=4 | pacommandnames\_open\_hardware\_manager=8 | pacommandnames\_reset\_run\_to\_previous\_step=4 | pacommandnames\_reset\_runs=2 |
| pacommandnames\_run\_bitgen=1 | pacommandnames\_run\_implementation=1 | pacommandnames\_simulation\_live\_restart=26 | pacommandnames\_simulation\_live\_run=428 |
| pacommandnames\_simulation\_objects\_window=1 | pacommandnames\_simulation\_relaunch=240 | pacommandnames\_simulation\_run\_behavioral=19 | pacommandnames\_src\_disable=3 |
| pacommandnames\_src\_enable=2 | partchooser\_parts=1 | paviews\_code=13 | paviews\_package=2 |
| paviews\_project\_summary=12 | paviews\_schematic=2 | programdebugtab\_program\_device=8 | programfpgadialog\_program=10 |
| progressdialog\_background=1 | progressdialog\_cancel=4 | projectnamechooser\_choose\_project\_location=2 | projecttab\_close\_design=1 |
| projecttab\_reload=2 | rdicommands\_custom\_commands=5 | rdicommands\_delete=2 | rdicommands\_properties=2 |
| rdicommands\_settings=5 | rdiviews\_waveform\_viewer=903 | settingsdialog\_project\_tree=4 | signaltreepanel\_signal\_tree\_table=5 |
| simulationliverunforcomp\_specify\_time\_and\_units=3 | simulationobjectspanel\_simulation\_objects\_tree\_table=84 | simulationscopespanel\_simulate\_scope\_table=57 | srcchooserpanel\_create\_file=4 |
| srcmenu\_ip\_hierarchy=4 | stalerundialog\_no=1 | syntheticagettingstartedview\_recent\_projects=11 | taskbanner\_close=1 |
| touchpointsurveydialog\_no=1 | touchpointsurveydialog\_remind\_me\_later=1 | waveformnametree\_waveform\_name\_tree=13 | waveformview\_goto\_last\_time=11 |
| waveformview\_goto\_time\_0=341 |

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| **java\_command\_handlers** | | | |
| addsources=6 | autoconnecttarget=7 | editdelete=2 | editproperties=2 |
| fliptoviewtaskimplementation=1 | launchprogramfpga=10 | newproject=2 | openhardwaremanager=22 |
| openproject=2 | openrecenttarget=12 | programdevice=2 | runbitgen=18 |
| runimplementation=20 | runschematic=3 | runsynthesis=6 | savefileproxyhandler=5 |
| setsourceenabled=5 | showview=2 | simulationrelaunch=224 | simulationrestart=26 |
| simulationrun=19 | simulationrunfortime=344 | toolssettings=5 | viewtaskimplementation=16 |
| viewtaskprogramanddebug=1 | viewtaskrtlanalysis=10 | viewtasksimulation=11 | viewtasksynthesis=3 |

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| **other\_data** | | | |
| guimode=12 |

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| **project\_data** | | | |
| constraintsetcount=1 | core\_container=false | currentimplrun=impl\_2 | currentsynthesisrun=[user-defined] |
| default\_library=xil\_defaultlib | designmode=RTL | export\_simulation\_activehdl=0 | export\_simulation\_ies=0 |
| export\_simulation\_modelsim=0 | export\_simulation\_questa=0 | export\_simulation\_riviera=0 | export\_simulation\_vcs=0 |
| export\_simulation\_xsim=0 | implstrategy=Vivado Implementation Defaults | launch\_simulation\_activehdl=0 | launch\_simulation\_ies=0 |
| launch\_simulation\_modelsim=0 | launch\_simulation\_questa=0 | launch\_simulation\_riviera=0 | launch\_simulation\_vcs=0 |
| launch\_simulation\_xsim=457 | simulator\_language=VHDL | srcsetcount=2 | synthesisstrategy=Vivado Synthesis Defaults |
| target\_language=VHDL | target\_simulator=XSim | totalimplruns=2 | totalsynthesisruns=2 |

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| **unisim\_transformation** |
| |  |  |  |  | | --- | --- | --- | --- | | **post\_unisim\_transformation** | | | | | bufg=1 | fdce=27 | fdpe=2 | gnd=2 | | ibuf=12 | ldce=15 | lut1=2 | lut2=8 | | lut3=10 | lut4=7 | lut5=3 | lut6=9 | | obuf=7 | vcc=2 | |
| |  |  |  |  | | --- | --- | --- | --- | | **pre\_unisim\_transformation** | | | | | bufg=1 | fdce=27 | fdpe=2 | gnd=2 | | ibuf=12 | ldce=15 | lut1=2 | lut2=8 | | lut3=10 | lut4=7 | lut5=3 | lut6=9 | | obuf=7 | vcc=2 | |

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| **report\_drc** |
| |  |  |  |  | | --- | --- | --- | --- | | **command\_line\_options** | | | | | -append=default::[not\_specified] | -checks=default::[not\_specified] | -fail\_on=default::[not\_specified] | -force=default::[not\_specified] | | -format=default::[not\_specified] | -messages=default::[not\_specified] | -name=default::[not\_specified] | -return\_string=default::[not\_specified] | | -ruledecks=default::[not\_specified] | -upgrade\_cw=default::[not\_specified] | -waived=default::[not\_specified] | |
| |  |  |  |  | | --- | --- | --- | --- | | **results** | | | | | pdrc-153=5 | plck-12=1 | zps7-1=1 | |

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| **report\_methodology** |
| |  |  |  |  | | --- | --- | --- | --- | | **command\_line\_options** | | | | | -append=default::[not\_specified] | -checks=default::[not\_specified] | -fail\_on=default::[not\_specified] | -force=default::[not\_specified] | | -format=default::[not\_specified] | -messages=default::[not\_specified] | -name=default::[not\_specified] | -return\_string=default::[not\_specified] | | -waived=default::[not\_specified] | |
| |  |  |  |  | | --- | --- | --- | --- | | **results** | | | | | timing-17=29 | timing-20=15 | |

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| **report\_power** |
| |  |  |  |  | | --- | --- | --- | --- | | **command\_line\_options** | | | | | -advisory=default::[not\_specified] | -append=default::[not\_specified] | -file=[specified] | -format=default::text | | -hier=default::power | -l=default::[not\_specified] | -name=default::[not\_specified] | -no\_propagation=default::[not\_specified] | | -return\_string=default::[not\_specified] | -rpx=[specified] | -verbose=default::[not\_specified] | -vid=default::[not\_specified] | | -xpe=default::[not\_specified] | |
| |  |  |  |  | | --- | --- | --- | --- | | **usage** | | | | | airflow=250 (LFM) | ambient\_temp=25.0 (C) | bi-dir\_toggle=12.500000 | bidir\_output\_enable=1.000000 | | board\_layers=8to11 (8 to 11 Layers) | board\_selection=medium (10"x10") | confidence\_level\_clock\_activity=Low | confidence\_level\_design\_state=High | | confidence\_level\_device\_models=High | confidence\_level\_internal\_activity=Medium | confidence\_level\_io\_activity=Low | confidence\_level\_overall=Low | | customer=TBD | customer\_class=TBD | devstatic=0.110066 | die=xc7z020clg484-1 | | dsp\_output\_toggle=12.500000 | dynamic=0.276254 | effective\_thetaja=11.5 | enable\_probability=0.990000 | | family=zynq | ff\_toggle=12.500000 | flow\_state=routed | heatsink=none | | i/o=0.103414 | input\_toggle=12.500000 | junction\_temp=29.5 (C) | logic=0.073511 | | mgtavcc\_dynamic\_current=0.000000 | mgtavcc\_static\_current=0.000000 | mgtavcc\_total\_current=0.000000 | mgtavcc\_voltage=1.000000 | | mgtavtt\_dynamic\_current=0.000000 | mgtavtt\_static\_current=0.000000 | mgtavtt\_total\_current=0.000000 | mgtavtt\_voltage=1.200000 | | mgtvccaux\_dynamic\_current=0.000000 | mgtvccaux\_static\_current=0.000000 | mgtvccaux\_total\_current=0.000000 | mgtvccaux\_voltage=1.800000 | | netlist\_net\_matched=NA | off-chip\_power=0.000000 | on-chip\_power=0.386321 | output\_enable=1.000000 | | output\_load=5.000000 | output\_toggle=12.500000 | package=clg484 | pct\_clock\_constrained=1.000000 | | pct\_inputs\_defined=0 | platform=nt64 | process=typical | ram\_enable=50.000000 | | ram\_write=50.000000 | read\_saif=False | set/reset\_probability=0.000000 | signal\_rate=False | | signals=0.099330 | simulation\_file=None | speedgrade=-1 | static\_prob=False | | temp\_grade=commercial | thetajb=7.4 (C/W) | thetasa=0.0 (C/W) | toggle\_rate=False | | user\_board\_temp=25.0 (C) | user\_effective\_thetaja=11.5 | user\_junc\_temp=29.5 (C) | user\_thetajb=7.4 (C/W) | | user\_thetasa=0.0 (C/W) | vccadc\_dynamic\_current=0.000000 | vccadc\_static\_current=0.020000 | vccadc\_total\_current=0.020000 | | vccadc\_voltage=1.800000 | vccaux\_dynamic\_current=0.002177 | vccaux\_io\_dynamic\_current=0.000000 | vccaux\_io\_static\_current=0.000000 | | vccaux\_io\_total\_current=0.000000 | vccaux\_io\_voltage=1.800000 | vccaux\_static\_current=0.010972 | vccaux\_total\_current=0.013149 | | vccaux\_voltage=1.800000 | vccbram\_dynamic\_current=0.000000 | vccbram\_static\_current=0.000497 | vccbram\_total\_current=0.000497 | | vccbram\_voltage=1.000000 | vccint\_dynamic\_current=0.216841 | vccint\_static\_current=0.008355 | vccint\_total\_current=0.225196 | | vccint\_voltage=1.000000 | vcco12\_dynamic\_current=0.000000 | vcco12\_static\_current=0.000000 | vcco12\_total\_current=0.000000 | | vcco12\_voltage=1.200000 | vcco135\_dynamic\_current=0.000000 | vcco135\_static\_current=0.000000 | vcco135\_total\_current=0.000000 | | vcco135\_voltage=1.350000 | vcco15\_dynamic\_current=0.000000 | vcco15\_static\_current=0.000000 | vcco15\_total\_current=0.000000 | | vcco15\_voltage=1.500000 | vcco18\_dynamic\_current=0.000000 | vcco18\_static\_current=0.000000 | vcco18\_total\_current=0.000000 | | vcco18\_voltage=1.800000 | vcco25\_dynamic\_current=0.000000 | vcco25\_static\_current=0.000000 | vcco25\_total\_current=0.000000 | | vcco25\_voltage=2.500000 | vcco33\_dynamic\_current=0.016817 | vcco33\_static\_current=0.001000 | vcco33\_total\_current=0.017817 | | vcco33\_voltage=3.300000 | vcco\_ddr\_dynamic\_current=0.000000 | vcco\_ddr\_static\_current=0.000000 | vcco\_ddr\_total\_current=0.000000 | | vcco\_ddr\_voltage=1.500000 | vcco\_mio0\_dynamic\_current=0.000000 | vcco\_mio0\_static\_current=0.000000 | vcco\_mio0\_total\_current=0.000000 | | vcco\_mio0\_voltage=1.800000 | vcco\_mio1\_dynamic\_current=0.000000 | vcco\_mio1\_static\_current=0.000000 | vcco\_mio1\_total\_current=0.000000 | | vcco\_mio1\_voltage=1.800000 | vccpaux\_dynamic\_current=0.000000 | vccpaux\_static\_current=0.010330 | vccpaux\_total\_current=0.010330 | | vccpaux\_voltage=1.800000 | vccpint\_dynamic\_current=0.000000 | vccpint\_static\_current=0.018172 | vccpint\_total\_current=0.018172 | | vccpint\_voltage=1.000000 | vccpll\_dynamic\_current=0.000000 | vccpll\_static\_current=0.003000 | vccpll\_total\_current=0.003000 | | vccpll\_voltage=1.800000 | version=2017.4 | |

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| **report\_utilization** |
| |  |  |  |  | | --- | --- | --- | --- | | **clocking** | | | | | bufgctrl\_available=32 | bufgctrl\_fixed=0 | bufgctrl\_used=1 | bufgctrl\_util\_percentage=3.13 | | bufhce\_available=72 | bufhce\_fixed=0 | bufhce\_used=0 | bufhce\_util\_percentage=0.00 | | bufio\_available=16 | bufio\_fixed=0 | bufio\_used=0 | bufio\_util\_percentage=0.00 | | bufmrce\_available=8 | bufmrce\_fixed=0 | bufmrce\_used=0 | bufmrce\_util\_percentage=0.00 | | bufr\_available=16 | bufr\_fixed=0 | bufr\_used=0 | bufr\_util\_percentage=0.00 | | mmcme2\_adv\_available=4 | mmcme2\_adv\_fixed=0 | mmcme2\_adv\_used=0 | mmcme2\_adv\_util\_percentage=0.00 | | plle2\_adv\_available=4 | plle2\_adv\_fixed=0 | plle2\_adv\_used=0 | plle2\_adv\_util\_percentage=0.00 | |
| |  |  |  |  | | --- | --- | --- | --- | | **dsp** | | | | | dsps\_available=220 | dsps\_fixed=0 | dsps\_used=0 | dsps\_util\_percentage=0.00 | |
| |  |  |  |  | | --- | --- | --- | --- | | **io\_standard** | | | | | blvds\_25=0 | diff\_hstl\_i=0 | diff\_hstl\_i\_18=0 | diff\_hstl\_ii=0 | | diff\_hstl\_ii\_18=0 | diff\_hsul\_12=0 | diff\_mobile\_ddr=0 | diff\_sstl135=0 | | diff\_sstl135\_r=0 | diff\_sstl15=0 | diff\_sstl15\_r=0 | diff\_sstl18\_i=0 | | diff\_sstl18\_ii=0 | hstl\_i=0 | hstl\_i\_18=0 | hstl\_ii=0 | | hstl\_ii\_18=0 | hsul\_12=0 | lvcmos12=0 | lvcmos15=0 | | lvcmos18=0 | lvcmos25=0 | lvcmos33=1 | lvds\_25=0 | | lvttl=0 | mini\_lvds\_25=0 | mobile\_ddr=0 | pci33\_3=0 | | ppds\_25=0 | rsds\_25=0 | sstl135=0 | sstl135\_r=0 | | sstl15=0 | sstl15\_r=0 | sstl18\_i=0 | sstl18\_ii=0 | | tmds\_33=0 | |
| |  |  |  |  | | --- | --- | --- | --- | | **memory** | | | | | block\_ram\_tile\_available=140 | block\_ram\_tile\_fixed=0 | block\_ram\_tile\_used=0 | block\_ram\_tile\_util\_percentage=0.00 | | ramb18\_available=280 | ramb18\_fixed=0 | ramb18\_used=0 | ramb18\_util\_percentage=0.00 | | ramb36\_fifo\_available=140 | ramb36\_fifo\_fixed=0 | ramb36\_fifo\_used=0 | ramb36\_fifo\_util\_percentage=0.00 | |
| |  |  |  |  | | --- | --- | --- | --- | | **primitives** | | | | | bufg\_functional\_category=Clock | bufg\_used=1 | fdce\_functional\_category=Flop & Latch | fdce\_used=27 | | fdpe\_functional\_category=Flop & Latch | fdpe\_used=2 | ibuf\_functional\_category=IO | ibuf\_used=12 | | ldce\_functional\_category=Flop & Latch | ldce\_used=15 | lut1\_functional\_category=LUT | lut1\_used=2 | | lut2\_functional\_category=LUT | lut2\_used=8 | lut3\_functional\_category=LUT | lut3\_used=10 | | lut4\_functional\_category=LUT | lut4\_used=7 | lut5\_functional\_category=LUT | lut5\_used=3 | | lut6\_functional\_category=LUT | lut6\_used=9 | obuf\_functional\_category=IO | obuf\_used=7 | |
| |  |  |  |  | | --- | --- | --- | --- | | **slice\_logic** | | | | | f7\_muxes\_available=26600 | f7\_muxes\_fixed=0 | f7\_muxes\_used=0 | f7\_muxes\_util\_percentage=0.00 | | f8\_muxes\_available=13300 | f8\_muxes\_fixed=0 | f8\_muxes\_used=0 | f8\_muxes\_util\_percentage=0.00 | | lut\_as\_logic\_available=53200 | lut\_as\_logic\_fixed=0 | lut\_as\_logic\_used=30 | lut\_as\_logic\_util\_percentage=0.06 | | lut\_as\_memory\_available=17400 | lut\_as\_memory\_fixed=0 | lut\_as\_memory\_used=0 | lut\_as\_memory\_util\_percentage=0.00 | | register\_as\_flip\_flop\_available=106400 | register\_as\_flip\_flop\_fixed=0 | register\_as\_flip\_flop\_used=29 | register\_as\_flip\_flop\_util\_percentage=0.03 | | register\_as\_latch\_available=106400 | register\_as\_latch\_fixed=0 | register\_as\_latch\_used=15 | register\_as\_latch\_util\_percentage=0.01 | | slice\_luts\_available=53200 | slice\_luts\_fixed=0 | slice\_luts\_used=30 | slice\_luts\_util\_percentage=0.06 | | slice\_registers\_available=106400 | slice\_registers\_fixed=0 | slice\_registers\_used=44 | slice\_registers\_util\_percentage=0.04 | | fully\_used\_lut\_ff\_pairs\_fixed=0.04 | fully\_used\_lut\_ff\_pairs\_used=5 | lut\_as\_distributed\_ram\_fixed=0 | lut\_as\_distributed\_ram\_used=0 | | lut\_as\_logic\_available=53200 | lut\_as\_logic\_fixed=0 | lut\_as\_logic\_used=30 | lut\_as\_logic\_util\_percentage=0.06 | | lut\_as\_memory\_available=17400 | lut\_as\_memory\_fixed=0 | lut\_as\_memory\_used=0 | lut\_as\_memory\_util\_percentage=0.00 | | lut\_as\_shift\_register\_fixed=0 | lut\_as\_shift\_register\_used=0 | lut\_ff\_pairs\_with\_one\_unused\_flip\_flop\_fixed=0 | lut\_ff\_pairs\_with\_one\_unused\_flip\_flop\_used=11 | | lut\_ff\_pairs\_with\_one\_unused\_lut\_output\_fixed=11 | lut\_ff\_pairs\_with\_one\_unused\_lut\_output\_used=8 | lut\_flip\_flop\_pairs\_available=53200 | lut\_flip\_flop\_pairs\_fixed=0 | | lut\_flip\_flop\_pairs\_used=16 | lut\_flip\_flop\_pairs\_util\_percentage=0.03 | slice\_available=13300 | slice\_fixed=0 | | slice\_used=17 | slice\_util\_percentage=0.13 | slicel\_fixed=0 | slicel\_used=8 | | slicem\_fixed=0 | slicem\_used=9 | unique\_control\_sets\_used=10 | using\_o5\_and\_o6\_fixed=10 | | using\_o5\_and\_o6\_used=9 | using\_o5\_output\_only\_fixed=9 | using\_o5\_output\_only\_used=0 | using\_o6\_output\_only\_fixed=0 | | using\_o6\_output\_only\_used=21 | |
| |  |  |  |  | | --- | --- | --- | --- | | **specific\_feature** | | | | | bscane2\_available=4 | bscane2\_fixed=0 | bscane2\_used=0 | bscane2\_util\_percentage=0.00 | | capturee2\_available=1 | capturee2\_fixed=0 | capturee2\_used=0 | capturee2\_util\_percentage=0.00 | | dna\_port\_available=1 | dna\_port\_fixed=0 | dna\_port\_used=0 | dna\_port\_util\_percentage=0.00 | | efuse\_usr\_available=1 | efuse\_usr\_fixed=0 | efuse\_usr\_used=0 | efuse\_usr\_util\_percentage=0.00 | | frame\_ecce2\_available=1 | frame\_ecce2\_fixed=0 | frame\_ecce2\_used=0 | frame\_ecce2\_util\_percentage=0.00 | | icape2\_available=2 | icape2\_fixed=0 | icape2\_used=0 | icape2\_util\_percentage=0.00 | | startupe2\_available=1 | startupe2\_fixed=0 | startupe2\_used=0 | startupe2\_util\_percentage=0.00 | | xadc\_available=1 | xadc\_fixed=0 | xadc\_used=0 | xadc\_util\_percentage=0.00 | |

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| **router** |
| |  |  |  |  | | --- | --- | --- | --- | | **usage** | | | | | actual\_expansions=194743 | bogomips=0 | bram18=0 | bram36=0 | | bufg=0 | bufr=0 | ctrls=10 | dsp=0 | | effort=2 | estimated\_expansions=66300 | ff=44 | global\_clocks=1 | | high\_fanout\_nets=0 | iob=19 | lut=33 | movable\_instances=107 | | nets=119 | pins=448 | pll=0 | router\_runtime=0.000000 | | router\_timing\_driven=1 | threads=2 | timing\_constraints\_exist=1 | |

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| **synthesis** |
| |  |  |  |  | | --- | --- | --- | --- | | **command\_line\_options** | | | | | -assert=default::[not\_specified] | -bufg=default::12 | -cascade\_dsp=default::auto | -constrset=default::[not\_specified] | | -control\_set\_opt\_threshold=default::auto | -directive=default::default | -fanout\_limit=default::10000 | -flatten\_hierarchy=default::rebuilt | | -fsm\_extraction=one\_hot | -gated\_clock\_conversion=default::off | -generic=default::[not\_specified] | -include\_dirs=default::[not\_specified] | | -keep\_equivalent\_registers=default::[not\_specified] | -max\_bram=default::-1 | -max\_bram\_cascade\_height=default::-1 | -max\_dsp=default::-1 | | -max\_uram=default::-1 | -max\_uram\_cascade\_height=default::-1 | -mode=default::default | -name=default::[not\_specified] | | -no\_lc=default::[not\_specified] | -no\_srlextract=default::[not\_specified] | -no\_timing\_driven=default::[not\_specified] | -part=xc7z020clg484-1 | | -resource\_sharing=default::auto | -retiming=default::[not\_specified] | -rtl=default::[not\_specified] | -rtl\_skip\_constraints=default::[not\_specified] | | -rtl\_skip\_ip=default::[not\_specified] | -seu\_protect=default::none | -sfcu=default::[not\_specified] | -shreg\_min\_size=default::3 | | -top=State\_Machine | -verilog\_define=default::[not\_specified] | |
| |  |  |  |  | | --- | --- | --- | --- | | **usage** | | | | | elapsed=00:00:33s | hls\_ip=0 | memory\_gain=536.855MB | memory\_peak=814.832MB | |

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| **xsim** |
| |  |  |  |  | | --- | --- | --- | --- | | **command\_line\_options** | | | | | -sim\_mode=default::behavioral | -sim\_type=default:: | |